In the Claims:

The claims are as follows:

1. (Previously Presented) An electronic device comprising:

a semiconductor substrate;

a transistor in said substrate, said transistor comprising functional gate conductors over a top surface of said substrate, each functional gate conductor having a gate length and a gate width and extending in a widthwise direction from a common spine, said common spine extending in a direction perpendicular to said widthwise direction, said functional gate conductors positioned substantially parallel to each other in said widthwise direction and periodically spaced apart a fixed distance in said direction substantially perpendicular to said widthwise direction; and

dummy gate conductors, each having a length and a width and extending in said widthwise direction, said dummy gate conductors positioned substantially parallel to each other in said widthwise direction and periodically spaced apart said fixed distance in said direction substantially perpendicular to said widthwise direction, said dummy gate conductors not positioned between adjacent functional gate conductors, said dummy gate conductors positioned adjacent to ends of said functional gate conductors, and said dummy gates positioned over a gate dielectric layer over a trench filled with an insulating layer formed in said semiconductor substrate.

2. (Previously Presented) The electronic device of claim 1, wherein said functional gate conductors include gate conductors of at least two different gate widths.

3. (Previously Presented) The electronic device of claim 1, wherein said dummy gate conductors include gate conductors of at least two different gate widths.

4. (Previously Presented) The electronic device of claim 1, wherein said dummy gate conductors and functional gate conductors have the same gate width.

5. (Previously Presented) The electronic device of claim 1, further comprising additional dummy gate conductors positioned adjacent to sides of one or more of said functional gate conductors in said widthwise direction.

6. (Original) The electronic device of claim 5, wherein said additional dummy gate conductors are the same width as one of said functional gate conductors.

7. (Previously Presented) The electronic device of claim 1, wherein the gate length of said functional gate conductors is a function of positive integer multiples of a minimum gate length of said functional gate conductors and of positive integer multiples of said fixed distance.

8. (Previously Presented) The electronic device of claim 1, wherein the gate length of said dummy gate conductors is a function of positive integer multiples of a minimum gate length of said functional gate conductors and of positive integer multiples of said fixed distance.

9. (Original) The electronic device of claim 1, further including source/drains formed in said substrate underneath and proximate to said functional gate conductors.

10. (Original) The electronic device of claim 1, further including N-wells, P-wells or both N-wells and P-wells formed in said substrate underneath and proximate to said functional gate conductors.

11. (Original) The electronic device of claim 1, further including a gate dielectric formed between said gate conductors and said substrate.

12. (Previously Presented) A method of fabricating an electronic device comprising:

providing a semiconductor substrate;

forming a transistor in said substrate, said transistor comprising functional gate conductors over a top surface of said substrate, each functional gate conductor having a gate length and a gate width and extending in a widthwise direction from a common spine, said common spine extending in a direction perpendicular to said widthwise direction, said functional gate conductors positioned substantially parallel to each other in said widthwise direction and periodically spaced apart a fixed distance in said direction substantially perpendicular to said widthwise direction; and

forming dummy gate conductors, each having a length and a width and extending in said widthwise direction, said dummy gate conductors positioned substantially parallel to each other in said widthwise direction and periodically spaced apart said fixed distance in said direction substantially perpendicular to said widthwise direction, said dummy gate conductors not

positioned between adjacent functional gate conductors, said dummy gate conductors positioned adjacent to ends of said functional gate conductors, and said dummy gates positioned over a gate dielectric layer over a trench filled with an insulating layer formed in said semiconductor substrate.

13. (Previously Presented) The method of claim 12, wherein said functional gate conductors include functional conductors of at least two different gate widths.

14. (Previously Presented) The method of claim 12, wherein said dummy gate conductors include dummy conductors of at least two different gate widths.

15. (Previously Presented) The method of claim 12, wherein said dummy gate conductors and functional gate conductors have the same gate width.

16. (Previously Presented) The method of claim 12, further comprising forming additional dummy gate conductor positioned adjacent to sides of one or more of said functional gate conductors and in said widthwise direction.

17. (Original) The method of claim 16, wherein said additional dummy gate conductors are the same width as one of said functional gate conductors.

18. (Previously Presented) The method of claim 12, wherein the gate length of said functional gate conductors is a function of positive integer multiples of a minimum gate length of said functional gate conductors and of positive integer multiples of said fixed distance.

19. (Previously Presented) The method of claim 12, wherein the gate length of said dummy gate conductors is a function of positive integer multiples of a gate minimum length of said functional gate conductors and of positive integer multiples of said fixed distance.

20. (Original) The method of claim 12, further including forming source/drains in said substrate underneath and proximate to said functional gate conductors.

21. (Original) The method of claim 12, further including forming N-wells, P-wells or both N-wells and P-wells in said substrate underneath and proximate to said functional gate conductors.

22. (Original) The method of claim 12, further including a forming a gate dielectric between said gate conductors and said substrate.

23. (Withdrawn) A method of designing a device having a gate length and a gate width comprising:

providing a design grid of gate shapes, each gate shape having a fixed width defined by opposite ends and extending in a widthwise direction, a useable fixed width less than said fixed width and a fixed length extending in a lengthwise direction, said lengthwise direction substantially perpendicular to said widthwise direction, said gate shapes arranged substantially

parallel to each other in said widthwise direction and periodically spaced apart a fixed distance in said lengthwise direction; and

forming a functional gate shape from one or more of said gate shapes.

24. (Withdrawn) The method of claim 23, wherein gate shapes and portions of gate shapes not used to form said functional gate shape are left in place as dummy gate shapes not connected to said functional gate shape.

25. (Withdrawn) The method of claim 23 further comprising, if said gate length is equal to said fixed length, connecting a whole number of gate shapes together along an end of each of said number of gate shapes, the number of gate shapes determined by dividing said gate width by said useable fixed width.

26. (Withdrawn) The method of claim 23 further comprising, if said gate length is greater than said fixed length, determining a minimum positive integer and a Previously Presented gate length such that said Previously Presented gate length is greater than said gate length and said Previously Presented gate length is equal to said minimum positive integer times the sum of said fixed length and said fixed distance.

27. (Withdrawn) The method of claim 26, further including determining a Previously Presented gate width by multiplying together the sum of said fixed length and said fixed distance, said minimum positive integer and said fixed gate width and dividing the result by said fixed gate length.

28. (Withdrawn) The method of claim 27, further including connecting a number gate shapes equal to said minimum positive integer of gate shapes together along an end of each of said number of gate shapes, each gate shape of said number of gates shapes having a width equal to said Previously Presented gate width.

29. (Withdrawn) The method of claim 23 further including, if said gate width divided by said useable gate length is less than 1, forming said functional gate from a gate shape of a length equal to said gate width.

30. (Previously Presented) The electronic device of claim 1, wherein two adjacent dummy gates are integrally connected in a "U" shaped pattern.

31. (Previously Presented) The electronic device of claim 30, wherein said two adjacent dummy gates are of different gate widths.

32. (Previously Presented) The method of claim 12, wherein two adjacent dummy gates are integrally connected in a "U" shaped pattern.

33. (Previously Presented) The method of claim 32, wherein said two adjacent dummy gates are of different gate widths.